

深圳市亿显国际科技有限公司 ShenZhen Yes-Display International Technology CO.,LTD.			4.3 寸液晶显示屏 <b>4.3 Inch LCD Display Screen</b>	
File NO.	YS-LCM-001	REV	A/01	<a href="http://www.yes-display.com">http://www.yes-display.com</a>

# SPECIFICATION

## FOR

**Module:YS-PB-RGB-MS01 V1.0**

Designed by	R&D Checked by	Quality Department by	Approved by

### Approval by Customer:

OK

NG, Problem survey

Approved By \_\_\_\_\_

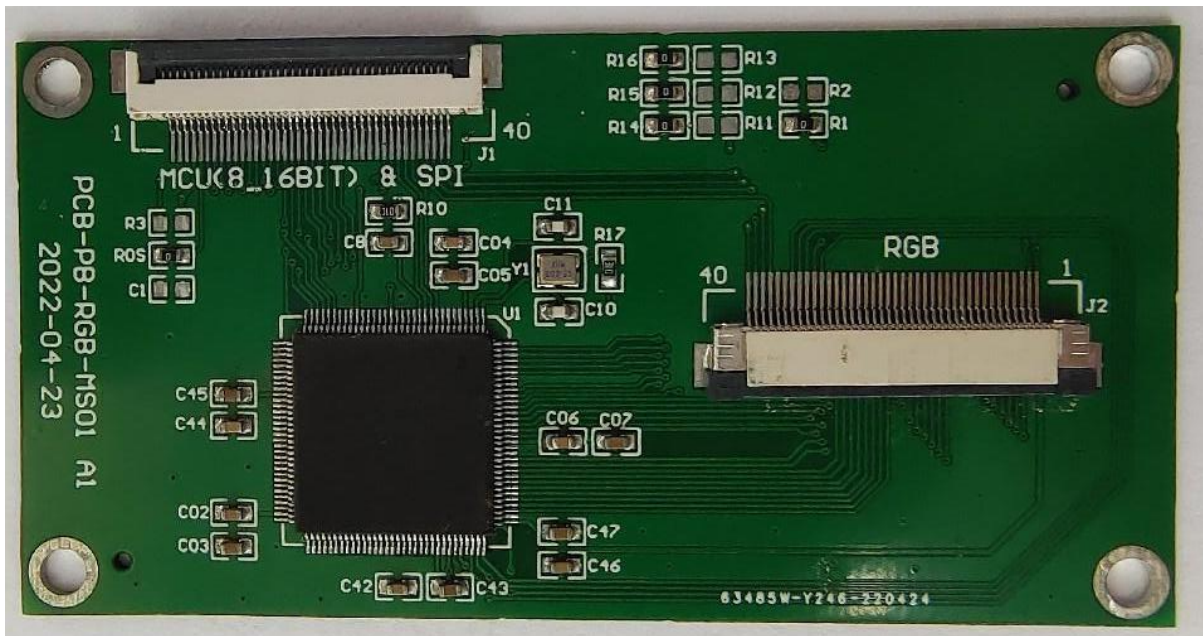


## Contents

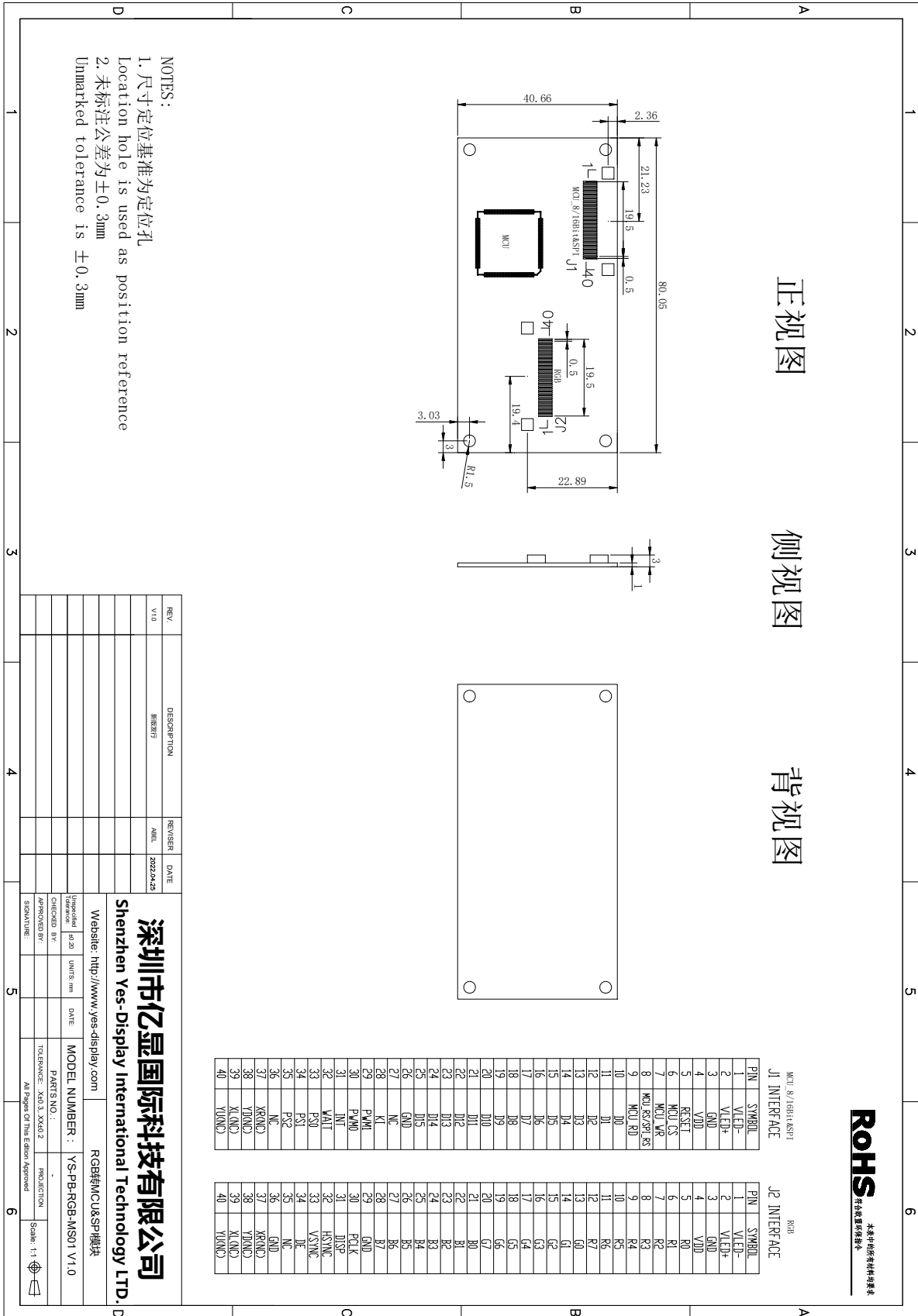
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## 1. Technical parameters

ITEM	STANDARD VALUES	UNITS
Driver IC	YS-7381	--
Module size	80.05(W)×40.66(H)×3.0(T)	mm
Interface	SPI&MCU	--
Weight	9	g



## 2. Outline Dimensions



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### 3. Input terminal Pin Assignment Description

#### 4.1 J1 INTERFACE(MCU\_8/16Bit&SPI)

PIN NO.	PIN NAME	DESCRIPTION
1	LEDK	LED backlight (Cathode).
2	LEDA	LED backlight (Anode).
3	GND	Ground for logic.
4	VDD	Power supply for voltage
5	RESET	Reset pin. Initializes the IC, when this signal is low. Must be reset after power is stable.
6	MCU_CS	Chip select input pin ("Low" enable).
7	MCU_WR	Write enable pin I80 parallel bus system interface;
8	MCU_RS/SPI_RS	Input pin for chip selection signal.
9	MCU_RD	Read enable pin I80 parallel bus system interface.
10-13	D0-D3	DATA BUS
14	D4/SPI_CS	DATA BUS Or spi Chip select input pin ( "Low" enable).
15	D5/SPI_SDO	DATA BUS Or spi Data OUTPUT
16	D6/SPI_SDA	DATA BUS Or Serial communication data input and output ,Internal pull low
17	D7/SPI_SCLK	DATA BUS Or Serial communication clock input, Internal pull low
18-25	D8-D15	DATA BUS.
26	GND	Ground for logic.
27	NC	NC
28	KI	Key-Matrix Data Pins
29	PWM1	PWM' s output signal. The output mode is decided by configuration register. This pin can be used as the control signal of TFT panel' s back light.
30	PWM0	
31	INT	Interrupt Output Signal
32	WAIT	Wait Output Signal

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33	PS0	<table border="1"> <thead> <tr> <th>PSM[2:0]</th> <th>Host I/F Mode</th> </tr> </thead> <tbody> <tr> <td>0 0 X</td> <td>8bits or 16bits 8080 Parallel Interface Mode</td> </tr> <tr> <td>0 1 X</td> <td>8bits or 16bits 6800 Parallel Interface Mode</td> </tr> <tr> <td>1 0 0</td> <td>3-Wire SPI Mode</td> </tr> <tr> <td>1 0 1</td> <td>4-Wire SPI Mode</td> </tr> <tr> <td>1 1 X</td> <td>I2C Mode</td> </tr> </tbody> </table>	PSM[2:0]	Host I/F Mode	0 0 X	8bits or 16bits 8080 Parallel Interface Mode	0 1 X	8bits or 16bits 6800 Parallel Interface Mode	1 0 0	3-Wire SPI Mode	1 0 1	4-Wire SPI Mode	1 1 X	I2C Mode
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1 1 X	I2C Mode													
34	PS1													
35	PS2													
36	NC	NC												
37	XR/NC	No connection												
38	YD/NC	No connection												
39	XL/NC	No connection												
40	YU/NC	No connection												

## 4.1 J2 INTERFACE(RGB)

PIN NO.	PIN NAME	DESCRIPTION
1	LEDK	LED backlight (Cathode).
2	LEDA	LED backlight (Anode).
3	GND	Ground for logic.
4	VDD	Power supply for voltage
5-12	R0-R7	Red Data.
13-20	G0-G7	Green Data.
21-28	B0-B7	Blue Data.
29	GND	Ground for logic.
30	PCLK	Dot clock signal input. Latching input data at its rising edge.
31	DISP	Display on/off.
32	HSYNC	Horizontal sync input. Negative polarity.
33	VSYNC	Vertical sync input. Negative polarity.
34	DE	Data enable input. Active high to enable the input data bus.

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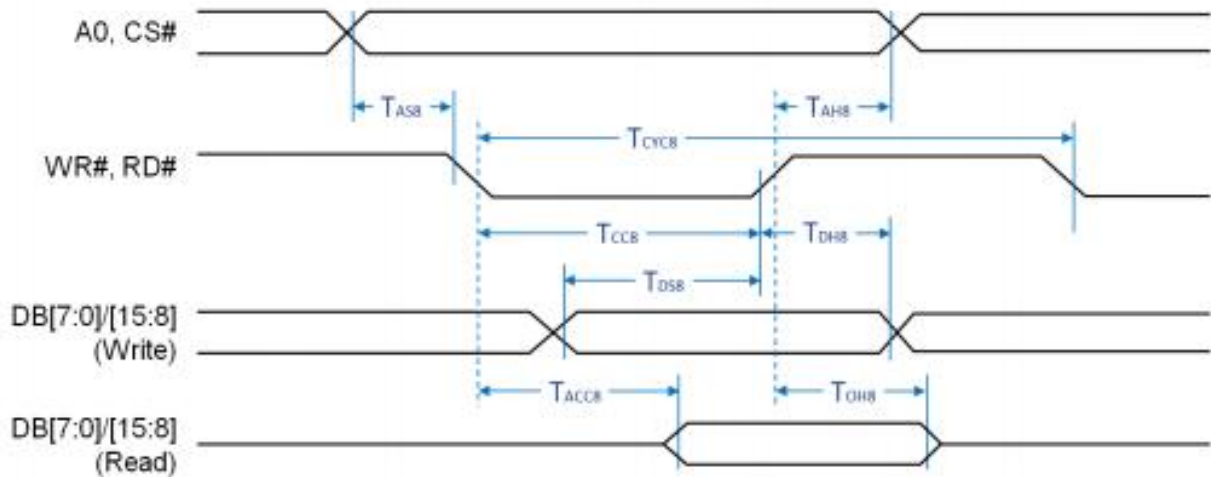
35	NC	No connection
36	GND	Ground for logic.
37	XR(NC)	No connection
38	YD(NC)	No connection
39	XL(NC)	No connection
40	YU(NC)	No connection



## 4. Timing Characteristics

### 7.1 TFT Timing Characteristics

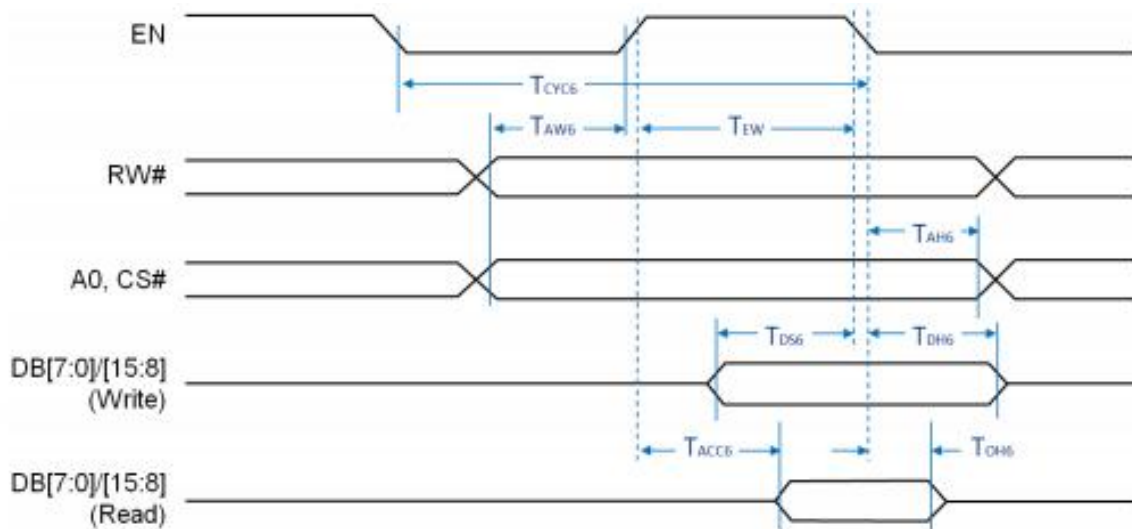
7.1.1 The followings are the application timing of 8080 parallel interface:



### 8080 Parallel Mode Interface Timing Parameter

Symbol	Parameter	Rating		Unit	Note
		Min.	Max.		
$T_{CYC8}$	Cycle Time	50	--	ns	tc is one system clock period: tc = 1/SYS_CLK
$T_{CC8}$	Strobe Pulse Width	20	--	ns	
$T_{AS8}$	Address Setup Time	0	--	ns	
$T_{AH8}$	Address Hold Time	10	--	ns	
$T_{DS8}$	Data Setup Time	20	--	ns	
$T_{DH8}$	Data Hold Time	10	--	ns	
$T_{ACC8}$	Data Output Access Time	0	20	ns	
$T_{OH8}$	Data Output Hold Time	0	20	ns	

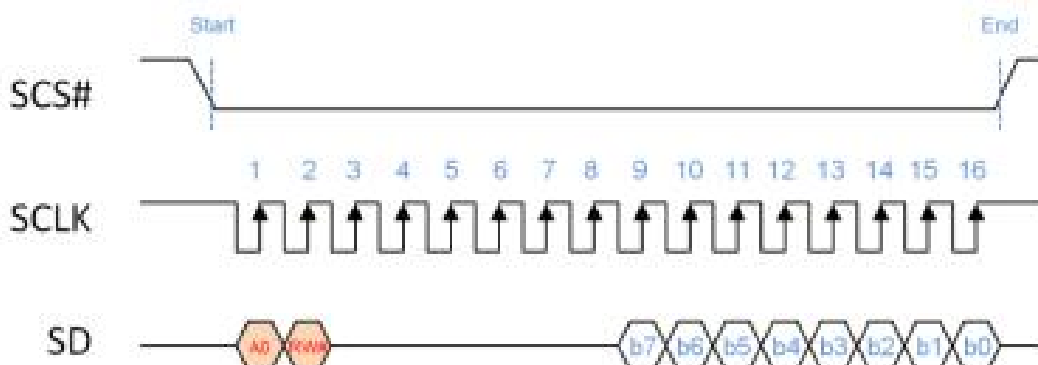
7.1.2 The followings are the application timing of 6800 parallel interface:



### 6800 Parallel Mode Interface Timing Parameter

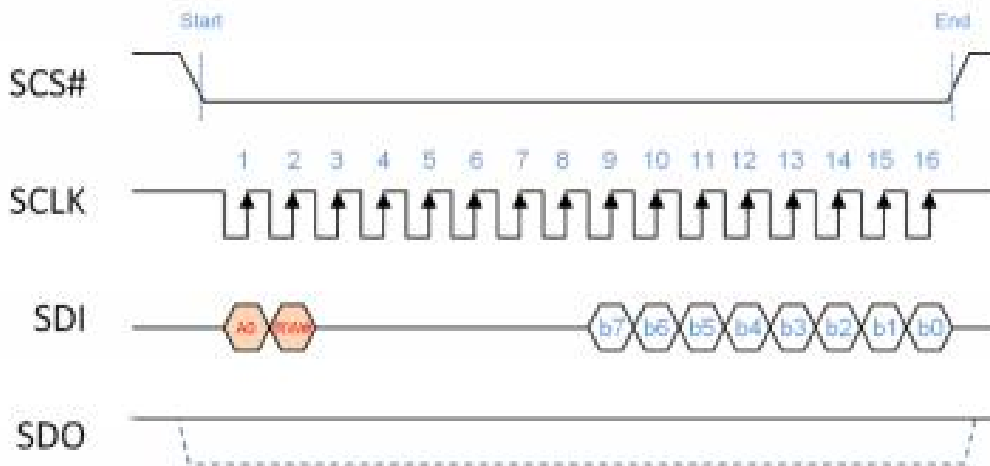
Symbol	Parameter	Rating		Unit	Note
		Min.	Max.		
$T_{CYCS}$	Cycle Time	50	--	ns	tc is one system clock period: tc = 1/SYS_CLK
$T_{EW}$	Strobe Pulse Width	20	--	ns	
$T_{AW6}$	Address Setup Time	0	--	ns	
$T_{AH6}$	Address Hold Time	10	--	ns	
$T_{DS6}$	Data Setup Time	20	--	ns	
$T_{DH6}$	Data Hold Time	10	--	ns	
$T_{ACC6}$	Data Output Access Time	0	20	ns	
$T_{OH6}$	Data Output Hold Time	0	20	ns	

### 7.1.3 The followings are the application timing of 3-Wire SPI parallel interface:

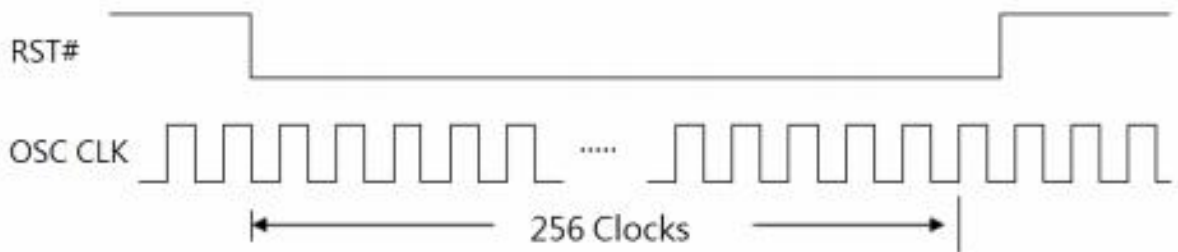


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**7.1.4 The followings are the application timing of 4-Wire SPI parallel interface:**



**7.1.5 Reset Timing Characteristics**



## 5. Reliability Test Conditions and Methods

The serial port screen has undergone a series of reliability tests: high and low temperature, ESD, pulse, radiation, touch life, etc., to ensure product quality, as shown in the following figure:

串口屏经过一系列的可靠性实验测试: 高低温, ESD, 脉冲, 辐射, 触摸寿命等测试, 确保产品品质, 如下图所示:

